

SYNC SEPARATOR DESIGN FOR TRANSISTOR TV RECEIVERS

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I. INTRODUCTION

A television receiver sync separator removes the synchronizing information from the received composite video signal and supplies the resultant signal to the horizontal and vertical oscillators. The process of sync separation is performed by limiting the signal level so that the sync pulses are isolated from the picture information. Transistors are particularly well suited for this because of their nonlinear or limiting transfer characteristics with large amplitude input signals.

The sync separator design discussed in this paper is part of a transistorized TV receiver using all silicon planar devices.

II. PRINCIPLE OF OPERATION

The sync separator schematic is shown in Fig. 1. It consists of an SE1001 silicon planar transistor in a common-emitter stage having zero forward bias. Base current will flow during the sync interval when a video signal of 2.5 to 3.0 volts, peak-to-peak, is applied to the input. This current produces a charge on capacitor C_1 , which discharges

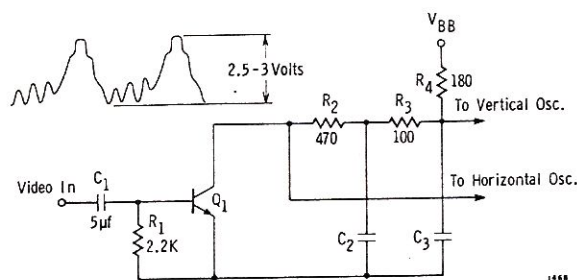


FIG. 1. Schematic diagram of sync separator.

through R_1 between pulses and the average voltage established at the base of transistor Q_1 is sufficient to produce cutoff during the time between sync signals. Q_1 is driven to the nonlinear regions by the sync pulses so that the collector swings between collector saturation and the voltage across capacitor C_2 . The collector signal, then, represents only the vertical and horizontal synchronizing pulses. The horizontal pulses are applied directly from the collector to the horizontal phase discriminator and the vertical pulses are integrated and fed to the vertical oscillator section.

III. DESIGN OF THE SYNC SEPARATOR

An equivalent circuit of the sync separator is shown in Fig. 2. It is divided into three sections: the video source; sync separation; and sync amplification and integration. The input or video source will first be considered.

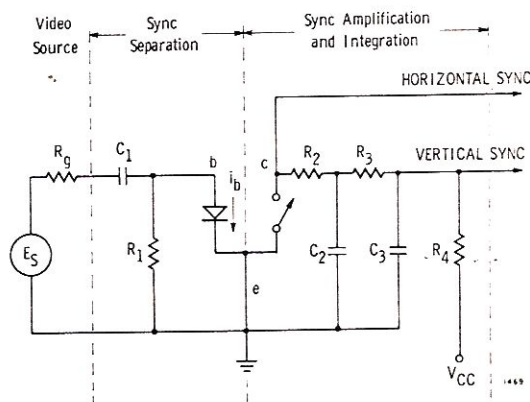


FIG. 2. Equivalent circuit of sync separator.

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The sync separator action that takes place in the input depends upon the resistance ratio

$$(R_g + R_1) / R_g.$$

The optimum ratio of R_1 to R_g as described in the Appendix (Eq. 8A) is 46.7 or $R_1 = 46.7 R_g$. Since the sync separator is driven from an emitter follower having an output resistance of 50 ohms, the value of R_1 is 2335 ohms.

The value of C_1 is found by allowing $R_1 C_1$ to equal the time period for 100 horizontal lines:

$$\begin{aligned} R_1 C_1 &= 100 t_L & (1) \\ C_1 &= 100 (63.5) (10^{-6}) / 2335 \\ &= 2.72 \mu f \end{aligned}$$

The amplitude of the horizontal sync pulses out of the sync separator is equal to the voltage across capacitor C_2 less the $V_{CE}(\text{sat})$ of transistor Q_1 . During the time not occupied by the vertical blanking interval, the voltage across capacitor C_2 is

$$E_{C2} = V_{CC} - (V_{CC} - V_{CE}(\text{sat})) \left(\frac{R_3 + R_4}{R_2 + R_3 + R_4} \right) \left(\frac{t_{HS}}{t_L} \right) \quad (2)$$

The values of resistors R_2 , R_3 , and R_4 are chosen to be compatible with the sync source resistance required by both the horizontal and vertical sweep oscillators. The following values were selected for a typical television receiver:

$$R_2 = 470 \text{ ohms}, R_3 = 100 \text{ ohms}, R_4 = 180 \text{ ohms}.$$

The load resistor, R_2 , is shunted by the load of the horizontal phase detector having a typical value of 1 kilohm; thus, R_2 is replaced by $R'_2 = 320$ ohms.

The collector-to-emitter switch closure time $t_{HS} = 4.5 \mu\text{sec}$ while the time between successive closure $t_L = 63.5 \mu\text{sec}$. It is assumed that $V_{CE}(\text{sat}) = 1$ volt. Substituting these values in Eq. 2, the voltage across capacitor C_2 is found

$$\begin{aligned} E_{C2} &= 12 - (12 - 1) \left(\frac{100 + 180}{320 + 100 + 180} \right) \left(\frac{4.5 \times 10^{-6}}{63.5 \times 10^{-6}} \right) \\ &= 11.6 \text{ volts} \end{aligned}$$

The resulting amplitude of output horizontal sync pulse is determined by subtracting the collector saturation voltage of Q_1 as follows:

$$E_{HS} = E_{C2} - V_{CE}(\text{sat}) = 10.6 \text{ volts} \quad (3)$$

The maximum collector current during the horizontal sync time, t_{HS} , is

$$I_C(\text{max}) = E_{HS} / R'_2 = 33 \text{ mA} \quad (4)$$

The minimum required value of forward-current transfer ratio, β , of the transistor is determined by the available base current under the limiting condition of the video signal which is given by the expression

$$\beta_{\min} = I_C(\text{max}) / i_b(\text{min}) \quad (5)$$

in which

$$i_b(\text{min}) = 0.215 E_{HS} / R_g \text{ as derived in the Appendix Eq. 14A.}$$

The lowest amplitude of input video signal has a peak-to-peak value of 2.5 volts; therefore, the horizontal sync pulse amplitude, taking the normal 25%, is a minimum of 0.625 volts. Solving for the minimum base current

$$i_b(\text{min}) = [0.215 \times 0.625] / 50 = 2.69 \text{ ma}$$

and substituting into Eq. 5 results in a value of $\beta_{\min}$ equal to 12.3.

This calculated value of $\beta_{\min}$ is defined at the previously assumed condition of $V_{CE}(\text{sat})$ equal to 1 volt and with $I_C(\text{max})$ equal to 33 ma. In the region of collector characteristics close to $V_{CE}(\text{sat})$ the forward current transfer ratio (β) falls off rapidly as V_{CE} is reduced. Also the condition varies from one transistor to another. Therefore for a particular transistor used in the sync separator, the $V_{CE}(\text{sat})$, $I_C(\text{max})$, and $\beta_{\min}$, being closely related, reach equilibrium values close to the calculated values. As a result, the amplitude of the

output horizontal sync pulse will vary from the calculated value. A typical sync separator, based on the above calculations, produced an output amplitude of 7 volts which provided adequate synchronization of the horizontal phase detector and oscillator.

The vertical sync pulse is formed by the integration of the separated serrated vertical pulse. The integration is produced by resistors R_2 and R_3 in combination with capacitors C_2 and C_3 . The first section of the integrator, consisting of resistor R_2 and capacitor C_2 , has a time constant approximately equal to the time interval of four serrated vertical pulses. If the time constant were made shorter, the amplitude of the horizontal sync pulse would be reduced to an unsuitable level. This is because the integrated vertical pulse subtracts from the collector supply voltage during the time interval. The expression for the time constant of the first section of the integrator, therefore, is

$$\begin{aligned} R_2 C_2 &= 4 t_{VS} = 4 (27 \times 10^{-6}) \\ &= 4 (27 \times 10^{-6}) / 470 = 0.23 \mu f \end{aligned} \quad (6)$$

The second integrator section is a low-pass filter comprised of resistor R_3 and capacitor C_3 for the purpose of reducing the serration ripples in the integrated vertical sync pulse. The vertical sync pulse output of the sync separator is taken from the junction of resistors R_2 and R_3 .

The noise performance of the sync separator can be improved by the addition of a noise switch. The operation of the switch is such that noise pulses, greater than a predetermined level, cutoff the emitter current of the sync separator. This action prevents the noise from charging the input time constant capacitance of the sync separator input which could produce a temporary loss of the separated sync. In addition, the noise pulses are prevented from appearing in the collector circuit by the cutoff of emitter current.

IV. CONCLUSION

The use of a single transistor for the sync separation function in a television receiver can meet the criteria of commercial practice for stable performance under widely varying signal conditions. Improvement of reception under high noise conditions can be achieved by the inclusion of a noise switch of conventional design. Best operation of a single transistor separator, which must supply large values of sync output, results when it is driven by a low impedance video source as described in Application Note APP-67. The sync separator design described was used in a complete transistorized television receiver having a 19" picture tube. Performance of this set was equal to top-of-the line vacuum-tube receivers.

Reference

1. Sidney Deutsch, "Theory and Design of Television Receivers", McGraw-Hill Publishing Co., 1951.

Acknowledgment

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APPENDIX

Analysis of the sync separator

Separation of sync pulses from the video signal is based upon amplitude discrimination where the discrimination level is automatically controlled by the input video signal.¹ The diode separation circuit of Fig. 1A performs this function.

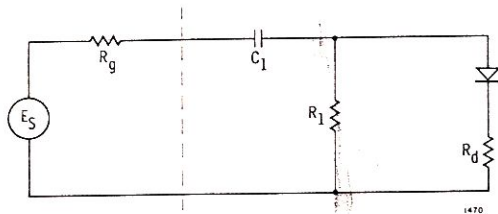
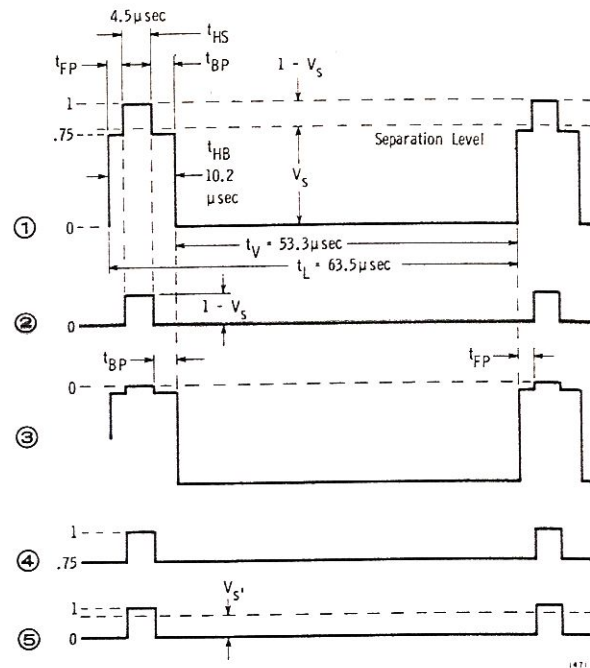


FIG. 1A. Schematic diagram of diode separator and signal source.

The video signal signal, E_S , shown in Fig. 2A, causes the capacitor C_1 to charge. The charging path is through the series resistance of the generator output and the diode which is in shunt with resistance R_1 during the time interval, t_{HS} . The capacitor C_1 then discharges through the source resistance, R_g , and the resistance R_1 during the time interval $t_L - t_{HS}$. By proper choice of the ratio of discharge path resistance to charge path resistance, an average voltage V_S will be established across the capacitor C_1 to determine the discrimination or separation level. Thus the diode current is caused to flow by the voltage difference between the peak sync level and the separation voltage level. As the diode in the actual circuit is the base-emitter diode of the sync separator transistor, the diode current results in a corresponding collector current flow that produces the output sync pulses.

For the purpose of analysis, it is assumed that the video input voltage contains 100% white level as shown in Fig. 2A(1). The coupling capacitor C_1 is sufficiently large so that voltage fluctuations across it, due to the charge and discharge currents, are negligible.



NOTE: V_S and V'_S are voltages normalized to the peak value of the respective waveforms.

FIG. 2A. Waveforms in sync separator.

The voltage that is effective in charging capacitor C_1 , as described previously, is shown in Fig. 2A (2). The resulting charge current for capacitor C_1 is

$$i_c = \left[1 - V_S \right] / \left[R_g + \frac{R_1 R_d}{R_1 + R_d} \right] \quad (1A)$$

The charge on capacitor C_1 as a result of i_c is

$$q_c = \int_0^{t_{HS}} i_c dt$$

substituting the expression for i_c , Eq. (1A), and integrating

$$q_c = \left[(1 - V_S) t_{HS} \right] / \left[R_g + \frac{R_1 R_d}{R_1 + R_d} \right] \quad (2A)$$

The discharge current for capacitor C_1 is the result of the voltage waveform as shown in Fig. 2A (3) appearing across the source resistance, R_g , in series with resistance R_1 . The resulting current flow has two different values during the discharge period. During the time intervals occupied by the front porch, t_{FP} , and the back porch, t_{BP} , the discharge current is

$$i_d = \frac{V_S - 0.75}{R_g + R_1} \left[\begin{array}{l} t_{FP} + t_{BP} \\ 0 \end{array} \right] \quad (3A)$$

During the time interval normally occupied by the video, the discharge current is

$$i'_d = \frac{V_S}{R_g + R_1} \left[\begin{array}{l} t_V \\ 0 \end{array} \right] \quad (4A)$$

The charge removed from capacitor C_1 by the total discharge current is

$$q_d = \int_0^{t_{FP} + t_{BP}} i_d dt + \int_0^{t_V} i'_d dt$$

substituting the expressions for i_d and i'_d , Eqs. (3A) and (4A) and integrating

$$q_d = \frac{(V_S - 0.75)(t_{FP} + t_{BP})}{R_g + R_1} + \frac{V_S t_V}{R_g + R_1} \quad (5A)$$

In order to maintain the average voltage V_S on capacitor C_1 the charge q_c and the reverse charge or discharge q_d must be equal

$$q_c = q_d$$

$$\frac{(1 - V_S) t_{HS}}{R_g + \frac{R_1 R_d}{R_1 + R_d}} = \frac{(V_S - 0.75)(t_{FP} + t_{BP})}{R_g + R_1} + \frac{V_S t_V}{R_g + R_1} \quad (6A)$$

From the above equation a solution is obtained for the ratio of discharge resistance to charge resistance:

$$\frac{R_g + R_1}{R_g + \frac{R_1 R_d}{R_1 + R_d}} = \frac{V_S(t_{FP} + t_{BP} + t_V)}{(1 - V_S) t_{HS}} - \frac{0.75(t_{FP} + t_{BP})}{(1 - V_S) t_{HS}}$$

The transistorized sync separator normally operates at rather low impedance levels so that the diode current is appreciable resulting in a forward resistance, R_D , that is considerably smaller than the source resistance R_g . Therefore, the resistance ratio equation simplifies to the following:

$$\frac{R_g + R_1}{R_g} \cong \frac{V_S(t_{FP} + t_{BP} + t_V)}{(1 - V_S) t_{HS}} - \frac{0.75(t_{FP} + t_{BP})}{(1 - V_S) t_{HS}}$$

The value of V_S should be somewhat greater than the 75% blacklevel to accommodate tolerances in the transmitted signal, therefore a reasonable value for V_S is 0.8. Using the standard values for the time intervals ($t_{FP} = 1.3 \mu\text{sec}$, $t_{BP} = 4.4 \mu\text{sec}$, $t_{HS} = 4.5 \mu\text{sec}$, $t_V = 53.3 \mu\text{sec}$) the final solution to the resistance ratio equation is

$$\frac{R_g + R_1}{R_g} \cong \frac{0.8(1.3 + 4.4 + 53.3) \times 10^{-6}}{(1 - 0.8) 4.5 \times 10^{-6}} - \frac{0.75(1.3 + 4.4) \times 10^{-6}}{(1 - 0.8) 4.5 \times 10^{-6}}$$

$$\cong 47.7 \quad (7A)$$

The value of R_1 is thus found to be

$$R_1 \cong 46.7 R_g \quad (8A)$$

The foregoing analysis was based on the limit condition of 100% white level during the time interval t_V . Normal television signals do not approach the limit condition and therefore the separation level is shifted in the direction of the peak sync level. However, sync separation still takes place although the amplitudes of the charge and discharge currents are decreased. For the limit condition shown in Fig. 2A(4) where the 75% or black level is approached for the time interval t_V , the charge and discharge currents are minimum. It is under this limit condition that the charge current, which is also the sync separator base current, must be sufficient to produce adequate change in the collector current.

It is necessary to determine the resistance ratio $(R_g + R_1)/R_g$ under the white limiting condition so that the separation level will remain beyond the video level of the video input signal. Having determined the resistance ratio, it is then necessary to define the transistor β for a given input signal level under the black limiting conditions.

By normalizing the waveform in Fig. 2A(4) to that shown in Fig. 2A(5) and describing a new separation level by the voltage V'_S the charging current i'_c is

$$i'_c = \frac{1 - V'_S}{R_g} \quad (\text{assumes } R_g \gg R_d) \quad (9A)$$

The resulting charge on capacitor C_1 is

$$\begin{aligned} q'_c &= \int_0^{t_{HS}} \frac{1 - V'_S}{R_g} dt \\ &= \frac{(1 - V'_S) t_{HS}}{R_g} \end{aligned} \quad (10A)$$

The discharge current i'_d is

$$i'_d = \frac{V'_S}{R_g + R_1} \quad (11A)$$

The charge removed from capacitor C_1 by i'_d is

$$\begin{aligned} q'_d &= \int_0^{t_L - t_{HS}} \frac{V'_S}{R_g + R_1} dt \\ &= \frac{V'_S (t_L - t_{HS})}{R_g + R_1} \end{aligned} \quad (12A)$$

The charge must be equal to the discharge in order to maintain the separation level V'_S

$$q'_c = q'_d$$

substituting (10A) and (12A) it becomes

$$\frac{(1 - V'_S) t_{HS}}{R_g} = \frac{V'_S (t_L - t_{HS})}{R_g + R_1}$$

and cross multiplying

$$\frac{R_g + R_1}{R_g} = \frac{V'_S (t_L - t_{HS})}{(1 - V'_S) t_{HS}}$$

Substituting the previously determined resistance ratio in the above equation the value of V'_S is obtained as follows:

$$\begin{aligned} V'_S &= \frac{47.7 t_{HS}}{t_L + 46.7 t_{HS}} \\ &= \frac{47.7 (4.5) 10^{-6}}{[63.5 + 46.7 (4.5)] 10^{-6}} \\ &= 0.785 \end{aligned} \quad (13A)$$

The charge current i'_c , which is also the minimum base current under the worst conditions, is as follows:

$$\begin{aligned} i_{b\min} &= i'_c = \frac{1 - V'_S}{R_g} \left(\frac{E_{HS}}{1} \right) \\ &= \frac{0.215 E_{HS}}{R_g} \end{aligned} \quad (14A)$$

Since the analysis was based on normalized voltage levels the factor E_{HS} , which is the horizontal sync pulse amplitude, is used to convert i'_c to the absolute value of current.

LIST OF SYMBOLS

E_{HS}	Amplitude of horizontal sync pulse
R_g	Video source output resistance
t_{BP}	Time duration of back porch ($4.4 \mu s$)
t_{FP}	Time duration of front porch ($1.3 \mu s$)
t_{HS}	Time duration of horizontal sync pulse ($4.5 \mu s$)
t_L	Time duration of one horizontal line ($63.5 \mu s$)
t_V	Time duration of video portion of horizontal line ($53.3 \mu s$)
V_{CC}	Collector supply voltage
$V_{CE} (sat)$	Collector-emitter saturation voltage
V'_S, V_S	Normalized value of separation-level voltage

ADDENDUM

An improvement in the sync separator can be effected by the addition of a $12 K\Omega$, $1/2 W$ resistor connected from the base of Q_1 (Fig. 1) to the $+12 V$ d-c supply. Without this resistor, the vertical oscillator may momentarily lose sync when the picture background scene rapidly changes from light to dark. This is a result of the d-c voltage component established across the input coupling capacitor (C_1) by the scenes having large white areas. The voltage is sufficient to effectively cut off the transistor when the input peak-to-peak voltage decreases with the beginning of a very dark scene. After sufficient capacitor discharge lowers the voltage to accommodate the dark scene level, vertical sync is reestablished. The added resistor in the base circuit decreases recovery time of the capacitor voltage so that synchronization is no longer lost.